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New concepts for crystal growth for photovoltaics

JMSerra[a]*

Faculdade de Ciências da Universidade de Lisboa/SESUL, Campo Grande Ed-C8,1749-016 Lisboa, Portugal

Abstract

The major barrier for PV penetration is cost. And the most important cost factor in silicon technology is the wafer (50% of the module cost). Although tremendous progress on cell processing has been reported in recent years, a much smaller evolution is seen on what should be the key point to address – the wafer. The ingot-slicing process is reaching its limits as the wafer thickness reduces in an effort to reduce costs. Kerf losses are putting a lower bound in this approach. To remain competitive we have to come up with new ideas for producing wafers in a way to overcome these limitations. In this paper we present some new concepts being developed in our laboratory that have one thing in common. They all are zero kerf loss processes. Considering that kerf loss can be higher than 50% of the final wafer material, of an already high valued material, this aspect is certainly important. Among these new techniques, we are developing processes for the growth of silicon directly into ribbons. They were conceived as continuous processes, based on a floating molten zone concept, to avoid impurity contamination during the crystallization. More singularly for continuous processes, they were conceived to allow for impurity segregation, making them interesting for less-pure silicon feedstock.

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Keywords: silicon, zero kerf loss, ribbons

1. Introduction

The major barrier for PV penetration is cost. And the most important cost factor in silicon technology is the wafer (50% of the module cost). Although tremendous progress on cell processing has been

* Corresponding author. Tel.: +351- 217500132; fax: +351-217500807
E-mail address: jmserra@fc.ul.pt.

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reported in recent years, a much smaller evolution is seen on what should be the key point to address – the wafer. In fact the silicon wafer is the basis of the dominant technology in the photovoltaics (PV) solar energy market. It accounts for the largest fraction of cost for (PV) industry: at ~0,69€/W, wafer cost is ~74% of solar cell cost, and ~50% of the solar module cost.

Its cost must decrease, if silicon based PV industry is to retain its dominance in a healthy market with growth rates of ~30%. Some decrease can still be accomplished with present wafer production technology. The ingot-slicing process is reaching its limits as the wafer thickness is reduced in an effort to reduce costs. Kerf losses are putting a lower bound in this approach, and looking into the future, it is obvious that a disruptive technology, capable of significantly decreasing costs while maintaining quality, is sorely needed. If we want PV to remain competitive we have to come up with new ideas for producing wafers in a way to overcome these limitations.

1.1. Cost structure of present solar cells

If one looks at the present cost/price structure of c-Si technology and at the evolution of technologies within each process, one may conclude that:

- Solar module fabrication still has a good margin for improvement, but incremental, given its very nature;
- Cell processing benefited from being the area where more academic research focused, and progressed tremendously.
- However, the most obvious area where a disruptive technology would be welcome is the wafer, since it accounts for ~74% of cell cost and ~50% of present module selling price.

2. Innovative techniques

In our laboratory, at the University of Lisbon, we are engaged in the development of several new processes for producing silicon wafers which have one point in common: they all are zero kerf loss concepts. Considering that kerf loss can be higher than 50% of the final wafer material, which already has a high value, makes this certainly important. One of the techniques addresses the challenges for obtaining very thin wafers. The other two techniques are designed for the growth of silicon directly into ribbons. The latter ones were conceived as continuous processes, based on a floating molten zone concept, to avoid impurity contamination during the crystallization. More singularly for continuous processes, they were conceived to allow for impurity segregation, making them interesting for less-pure silicon feedstock.

2.1. SlimCut

It is known that solar cell conversion efficiency will increase, upon reduction of the wafer thickness, peaking at a 55 microns thick wafer [1]. The SLIM-Cut technique, developed at IMEC(Belgium) relies on thermo-mechanical treatments: a high stress field is applied to a silicon wafer so that a crack propagates in the silicon substrate parallel to the surface at a given depth [2]. The top silicon layer is separated from the parent substrate and processed into a solar cell. The parent substrate can be re-used. With this process 50 micron thick wafers can be obtained. The choice of the stress inducing layer is extremely important: (1) the interfacial strength has to be high enough for the crack to grow in the Si lattice, (2) the metal

migration has to be limited in order not to compromise the PV conversion efficiency, and (3) the deposition method of the stressing layer should be compatible with PV cell processing.

2.2. EZ-Ribbon

The main point behind this concept is the decrease of the semiconductor resistivity with increasing temperature. If we apply an electric current in a semiconductor slab, the current flow lines will tend to concentrate in the hotter regions, with lower resistivity, thus creating stronger temperature gradients that will further concentrate the current lines. A positive feedback effect is thus created: the rise in temperature leads to local higher electric conductivity and lower thermal conductivity, decreasing heat losses from that region. As a result the electric current lines will concentrate in the hotter regions of the semiconductor. Above a critical current Ic, the rise in temperature will lead to the creation of a molten zone [3].

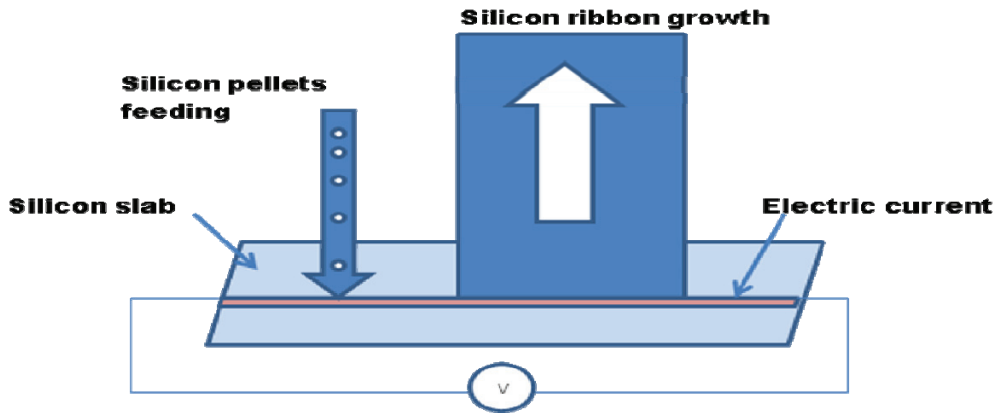

Fig 1 Concept idea of EZ-Ribbon process.

2.3. Silicon on Dust Substrate (SDS)

In the SDS process (see Fig 2) a layer of silicon dust, obtained from high purity gaseous feedstock, is placed on a quartz plate, acting both as a place for deposition and as a "sacrificial detachment layer". Secondly, a thick film is deposited on the bedding layer by fast CVD, at temperatures around 800 C and atmospheric pressure. Finally, the detached free standing ribbon is sprayed with a solution with boric acid and it is recrystallised by a floating molten zone (ZMR - Zone Melting Recrystallization) technique [4].

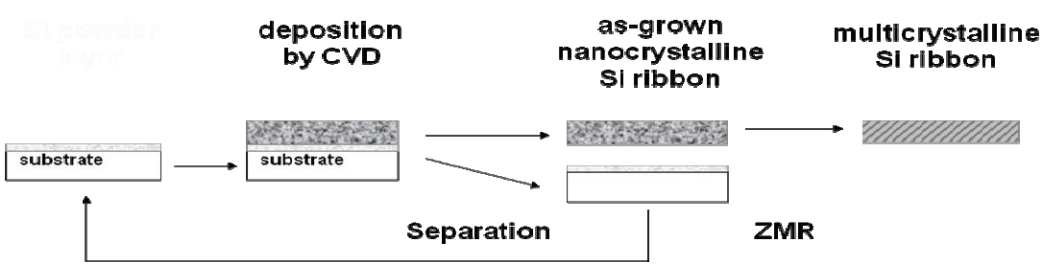

Fig 2 Flow-chart of the core of the SDS process.

The use of ZMR has two advantages: increase in crystal quality while avoiding impurity contamination. The doping is achieved by sprayed boric acid over the pre-ribbon surface prior to the crystallization step.

As a process the SDS has the following advantages: (1) no substrate (therefore no cost associated with it and no contamination); (2) low thermal budget (ambient pressure, low temperature CVD); (3) high quality and self-standing crystalline silicon sheet (float zone crystallization, no contact with foreign materials).

3. Results and discussion

The three approaches under study can be seen in the context of the silicon based technology in Fig 3. Note that ribbon technology also is a zero kerf loss one since no wafering is needed.

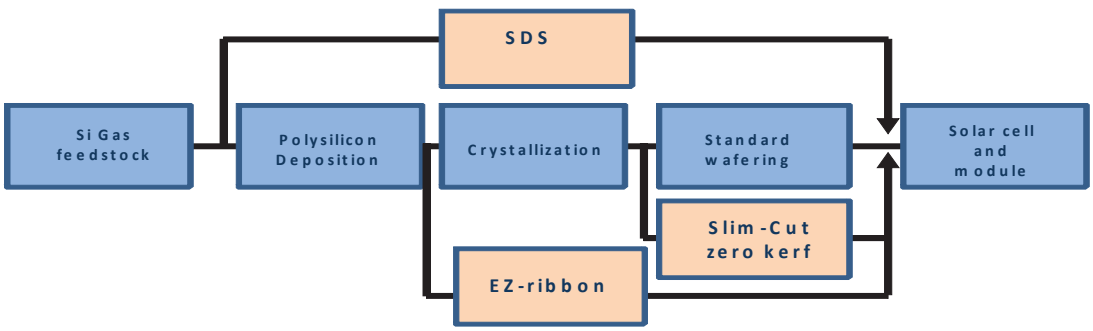

Fig 3 Relationship between the three explored alternative paths and present dominant c-Si technology.

The work on Slim-Cut development in which we are collaborating is part of IMEC's effort to develop silicon based thin film crystalline solar cells [5]. Slim-Cut wafers of 25 cm^2 have already been obtained, and solar cells with 1 cm^2 were demonstrated [6]. An important aspect in this process is the amount of mechanical stress that is needed to achieve the lift-off of the thin layer. From defect etching it has been found the current amount of defect density in the foils amounts to $10^7 cm^{-2}$[7].

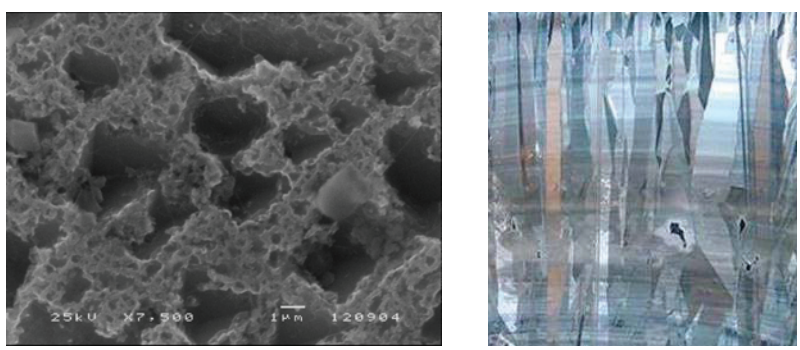

Fig 4 (a) SEM picture of an SDS pre-ribbon. (b) SDS final ribbon, 3 cm wide and 300 µm thick.

Ribbon technologies have a very interesting potential for low cost wafers since there is no need for wafering, providing this way significant cost reductions in materials costs. However, existing techniques rely on the existence of a crucible or die or a foreign substrate. Impurity contamination is a major limiting factor in those existing techniques. The two ribbons processes described above don't have these limitations. They are based on the floating zone method, known to be the most effective process in terms of avoiding impurity contamination, because there is neither a crucible nor a foreign substrate. Minority carrier lifetime measurements in SDS ribbons give typically values slightly above 3 μs [8].

The results obtained so far have demonstrated the feasibility of the alternative paths being studied and their potential for the achievement of the major goal of the PV industry – cost reduction of solar electricity.

Acknowledgements

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